REMARKS

Claims 1-11 remain for consideration. The allowability of claims 7-9 is acknowledged. All claims are thought to be allowable over the cited art.

The office action fails to establish that claims 1-5 are anticipated under 35 U.S.C. 102(b) by U.S. Patent No. 6,031,473 to Kubinec.

To anticipate claim 1, Kubinec must teach all the limitations of the claimed invention. In particular, Kubinec must be shown to teach "a first interface," as an illustration of support from FIGs. 2A/B of the specification, transmit interface 134, "that receives a first set of data," as an illustration , data 138, "from the data source," as an illustration, data source 140, "at a second data rate and delivers a second set of data," as an illustration, data 136, "to the serializer," as an illustration, serializer 132, "at the first data rate." Furthermore, Kubinec must be shown to teach that "the second data rate [is] lower than the first data rate when the control signal," as an illustration, select speed 146, "is at the first state and the second rate [is the] same as the first data rate when the control signal is at the second state" as at least set forth by Applicant's claim 1.

The Office Action intimates that input register 40 of Kubinec corresponds to the first interface as recited in Applicant's claim 1, since input register 40 receives input data, TDATA, from a data source and provides output data, TD1-TD5, to serializer 30. Kubinec, however, does not appear to teach that TDATA is received by input register 40 from a data source at the second data rate, nor that TD1-TD5 as provided by input register 40, is transferred to serializer 30 at the first or the second data rate, depending upon the state of a control signal.

According to the Office Action, Kubinec performs an increase in the information data rate by using a clock multiplier. (See column 4, lines 46-65.) This passage, however, appears to teach that the information rate is controlled via the frequency of the clock signal supplied to the serializer. Kubinec, however, appears to be silent as to the controllability of the information rate via an interface (input register 40) that supplies data (TD1-TD5) to the serializer (30) at first and second data rates based upon first and second states of a control signal.

In particular, Kubinec seems to be silent as to the control signal that is to be received by input register 40, which is then to be effective to switch the output data rate from input register 40 between first and second data rates in response to first and second states of the control signal. However, no such control signal is apparently received by input register 40 and the only other signal received by input register 40 seems to be signal DL, which appears to latch the first set of data, TDATA, to the second set of data, TD1-TD5, at the rising edge of signal DL. (See column 3, line 66, to column 4, line 6, and FIG. 3). Thus, Kubinec appears to be deficient as to the controllability of the output data rate from input register 40 to serializer 30, which is in contradistinction to Applicant's claim 1. Applicant respectfully submits, therefore, that claim 1 patentably distinguishes over Kubinec and is in condition for allowance.

To anticipate claim 2, Kubinec must be further shown to teach that the first interface comprises "a circuit for generating a first clock signal," as an example of support from FIGs. 2A/B of the specification, i/f clock 144, "based on the reference clock signal," for example, REFCLK 142, "the first clock signal being used by the data source," for example, data source 140, "to deliver the first set of data," for example, data 138, "to the first interface," for example, transmit interface 134, "the first clock signal having a lower frequency than the reference clock signal when the control signal," for example, select speed 146, "is at the first state."

As discussed above, the Office Action intimates that input register 40 of Kubinec corresponds to Applicant's first interface as at least set forth in claim 1. Input register 40, however, does not appear to provide a clock signal to a data source, which is then used by the data source to deliver the data to the first interface. Input register 40, on the other hand, appears to only provide output data, TD1-TD5, to serializer 30 in response to a rising edge of signal DL. (See column 3, line 66, to column 4, line 6, and FIG. 3). As such, input register 40 appears to be ineffective to control the data rate of data, TDATA, as received from a data source, which is in contradistinction to Applicant's claim 2. Applicant respectfully submits, therefore, that claim 2 patentably distinguishes over Kubinec and is in condition for allowance.

Dependent Claims 3-5, which are dependent from independent claim 1 and dependent claim 2, are also rejected under 35 U.S.C. §102(b) as being unpatentable

over Kubinec. While Applicant does not acquiesce to the particular rejections to these dependent claims, it is understood that these rejections are now moot in view of the remarks made in connection with independent claim 1 and dependent claim 2. These dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from Kubinec. Therefore, dependent claims 3-5 are also in condition for allowance.

The office action fails to establish that claims 6, 10, and 11 are unpatentable over Kubinec under 35 U.S.C. 103(a).

To establish *prima facie* obviousness of a claimed invention, the Examiner has the burden of proving that three basic criteria are met. First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. All three of these criteria must be met in order to support a finding of *prima facie* obviousness of a claimed invention. (See MPEP § 2142).

Concerning the third criteria, which must be met to establish *prima facie* obviousness of a claimed invention, Applicant respectfully submits that Kubinec fails to teach or suggest all the claim limitations of Applicant's claim 1 as discussed above. Consequently, since claims 6, 10, and 11 include all of the limitations of claim 1 and any intervening claims, and recite additional features which further distinguish these claims from Kubinec, Applicant respectfully submits that the Office Action fails as to the third criteria to establish *prima facie* obviousness of claims 6, 10, and 11. Applicant submits, therefore, that claims 6, 10, and 11 are also patentable over Kubinec and are in condition for allowance.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patent, Washington, D.C. 20231, on December 29, 2005.

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